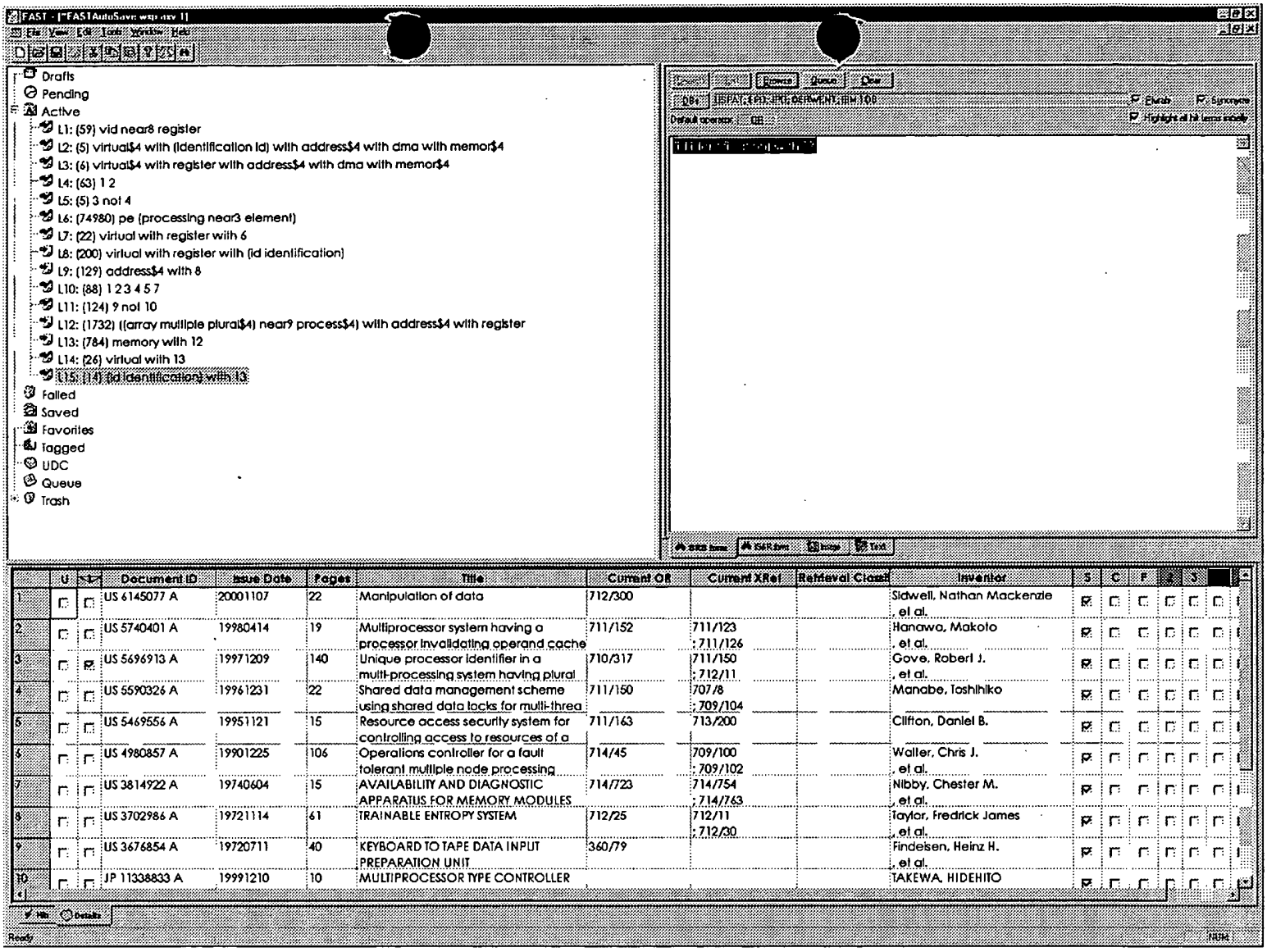
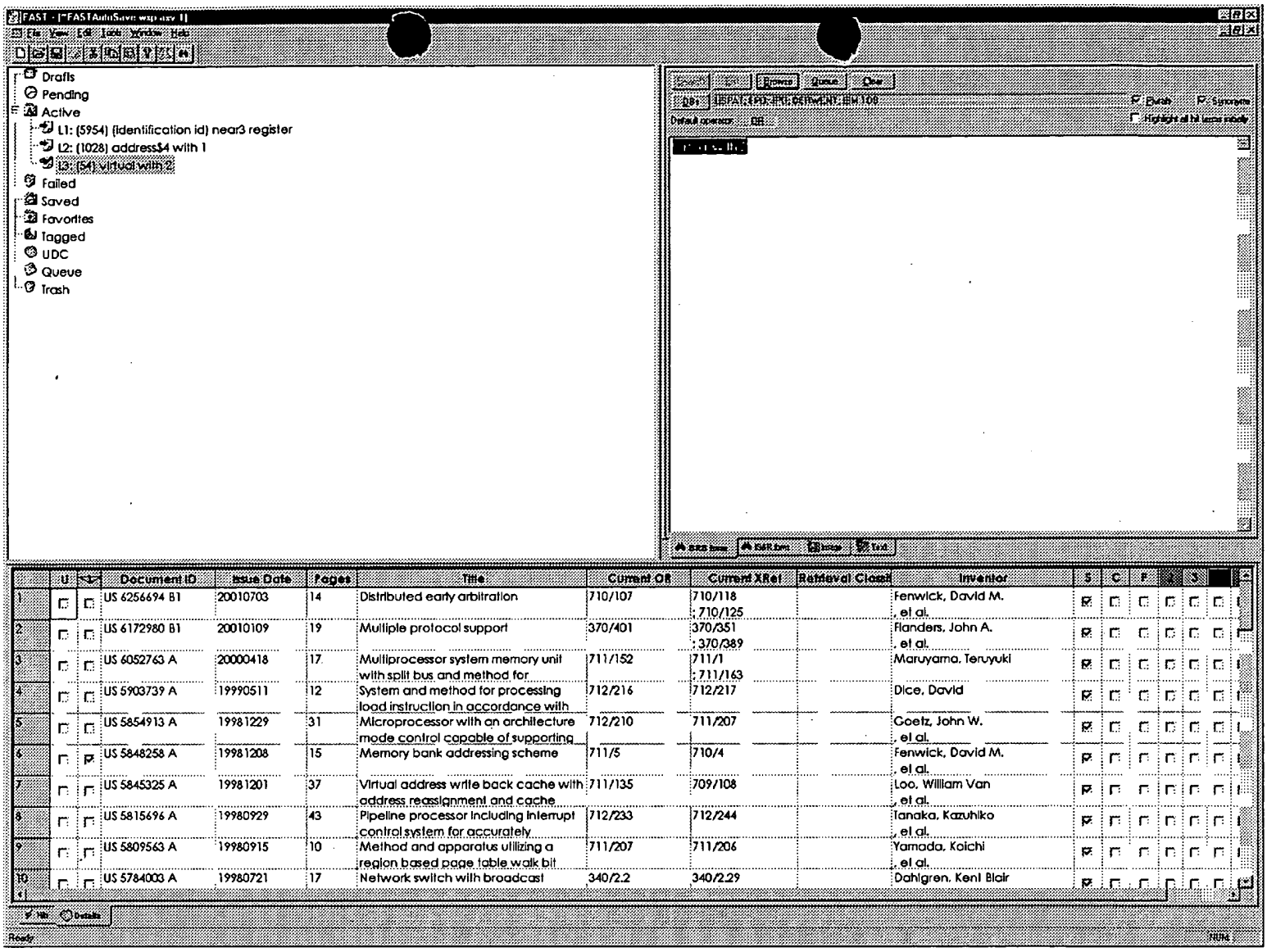


	U	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Class	Inventor	S	C	F	S	S
1	☐	US 6145077 A	20001107	22	Manipulation of data	712/300			Sidwell, Nathan Mackenzie , et al.	☑	☐	☐	☐	☐
2	☐	US 5740401 A	19980414	19	Multiprocessor system having a processor invalidating operand cache	711/152	711/123 ; 711/126		Hanawa, Makoto , et al.	☑	☐	☐	☐	☐
3	☐	US 5696913 A	19971209	140	Unique processor identifier in a multi-processing system having plural	710/317	711/150 ; 712/11		Gove, Robert J. , et al.	☑	☐	☐	☐	☐
4	☐	US 5590326 A	19961231	22	Shared data management scheme using shared data locks for multi-threa	711/150	707/8 ; 709/104		Manabe, Toshihiko	☑	☐	☐	☐	☐
5	☐	US 5469556 A	19951121	15	Resource access security system for controlling access to resources of a	711/163	713/200		Clifton, Daniel B.	☑	☐	☐	☐	☐
6	☐	US 4980857 A	19901225	106	Operations controller for a fault tolerant multiple node processing	714/45	709/100 ; 709/102		Walter, Chris J. , et al.	☑	☐	☐	☐	☐
7	☐	US 3814922 A	19740604	15	AVAILABILITY AND DIAGNOSTIC APPARATUS FOR MEMORY MODULES	714/723	714/754 ; 714/763		Nibby, Chester M. , et al.	☑	☐	☐	☐	☐
8	☐	US 3702986 A	19721114	61	TRAINABLE ENTROPY SYSTEM	712/25	712/11 ; 712/30		Taylor, Fredrick James , et al.	☑	☐	☐	☐	☐
9	☐	US 3676854 A	19720711	40	KEYBOARD TO TAPE DATA INPUT PREPARATION UNIT	360/79			Findeisen, Heinz H. , et al.	☑	☐	☐	☐	☐
10	☐	JP 11338833 A	19991210	10	MULTIPROCESSOR TYPE CONTROLLER				TAKEWA, HIDEHITO	☑	☐	☐	☐	☐



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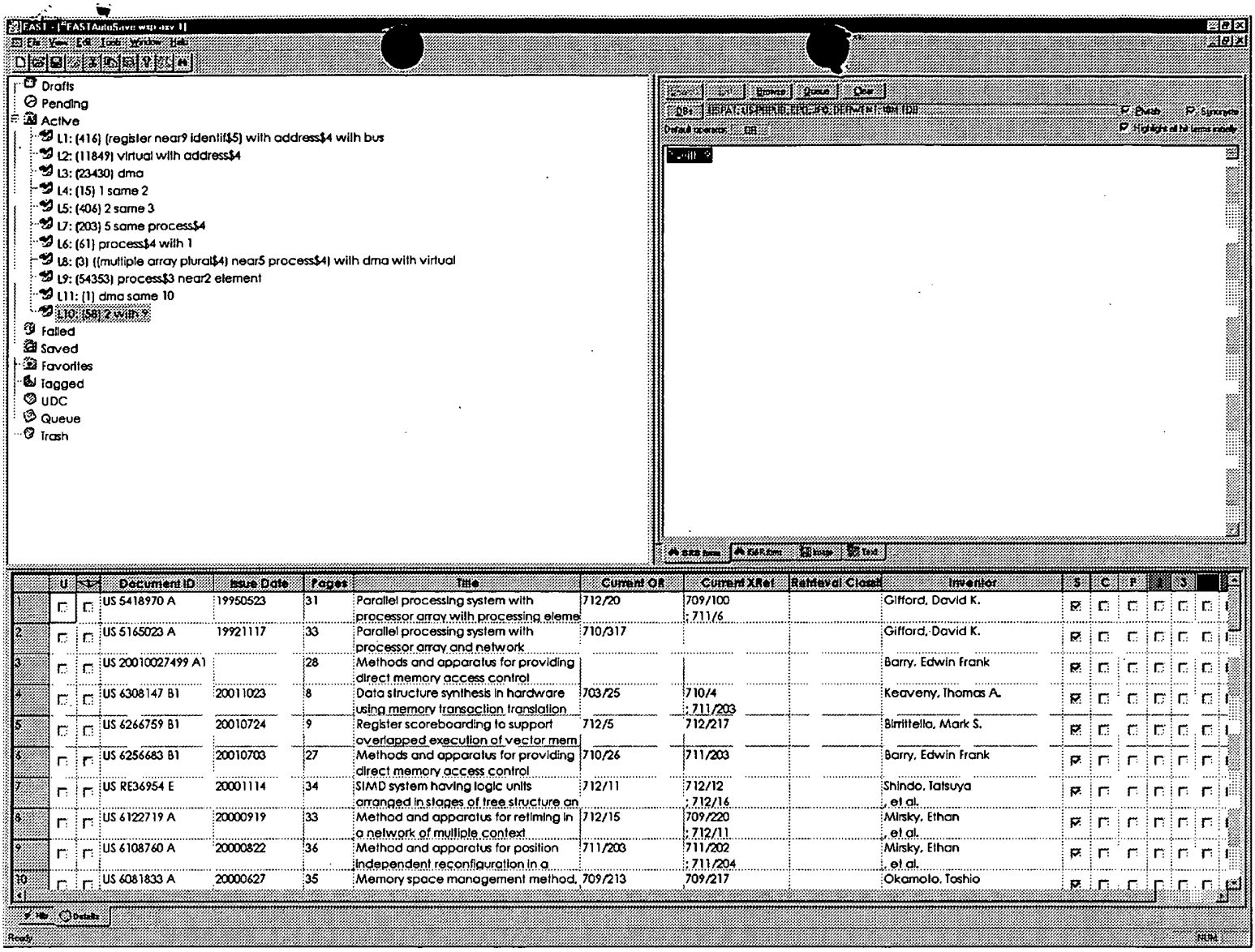
1	☐	☐	US 6256694 B1	20010703	14	Distributed early arbitration	710/107	710/118 ; 710/125		Fenwick, David M. , et al.	☑	☐	☐	☐	☐	☐
2	☐	☐	US 6172980 B1	20010109	19	Multiple protocol support	370/401	370/351 ; 370/389		Flanders, John A. , et al.	☑	☐	☐	☐	☐	☐
3	☐	☐	US 6052763 A	20000418	17	Multiprocessor system memory unit with split bus and method for	711/152	711/1 ; 711/163		Maruyama, Teruyuki	☑	☐	☐	☐	☐	☐
4	☐	☐	US 5903739 A	19990511	12	System and method for processing load instruction in accordance with	712/216	712/217		Dice, David	☑	☐	☐	☐	☐	☐
5	☐	☐	US 5854913 A	19981229	31	Microprocessor with an architecture mode control capable of supporting	712/210	711/207		Goetz, John W. , et al.	☑	☐	☐	☐	☐	☐
6	☐	☑	US 5848258 A	19981208	15	Memory bank addressing scheme	711/5	710/4		Fenwick, David M. , et al.	☑	☐	☐	☐	☐	☐
7	☐	☐	US 5845325 A	19981201	37	Virtual address write back cache with address reassignment and cache	711/135	709/108		Loo, William Van , et al.	☑	☐	☐	☐	☐	☐
8	☐	☐	US 5815696 A	19980929	43	Pipeline processor including interrupt control system for accurately	712/233	712/244		Tanaka, Kazuhiko , et al.	☑	☐	☐	☐	☐	☐
9	☐	☐	US 5809563 A	19980915	10	Method and apparatus utilizing a region based page table walk bit	711/207	711/206		Yamada, Koichi , et al.	☑	☐	☐	☐	☐	☐
10	☐	☐	US 5784003 A	19980721	17	Network switch with broadcast	340/2.2	340/2.29		Dahlgren, Kent Blair	☑	☐	☐	☐	☐	☐



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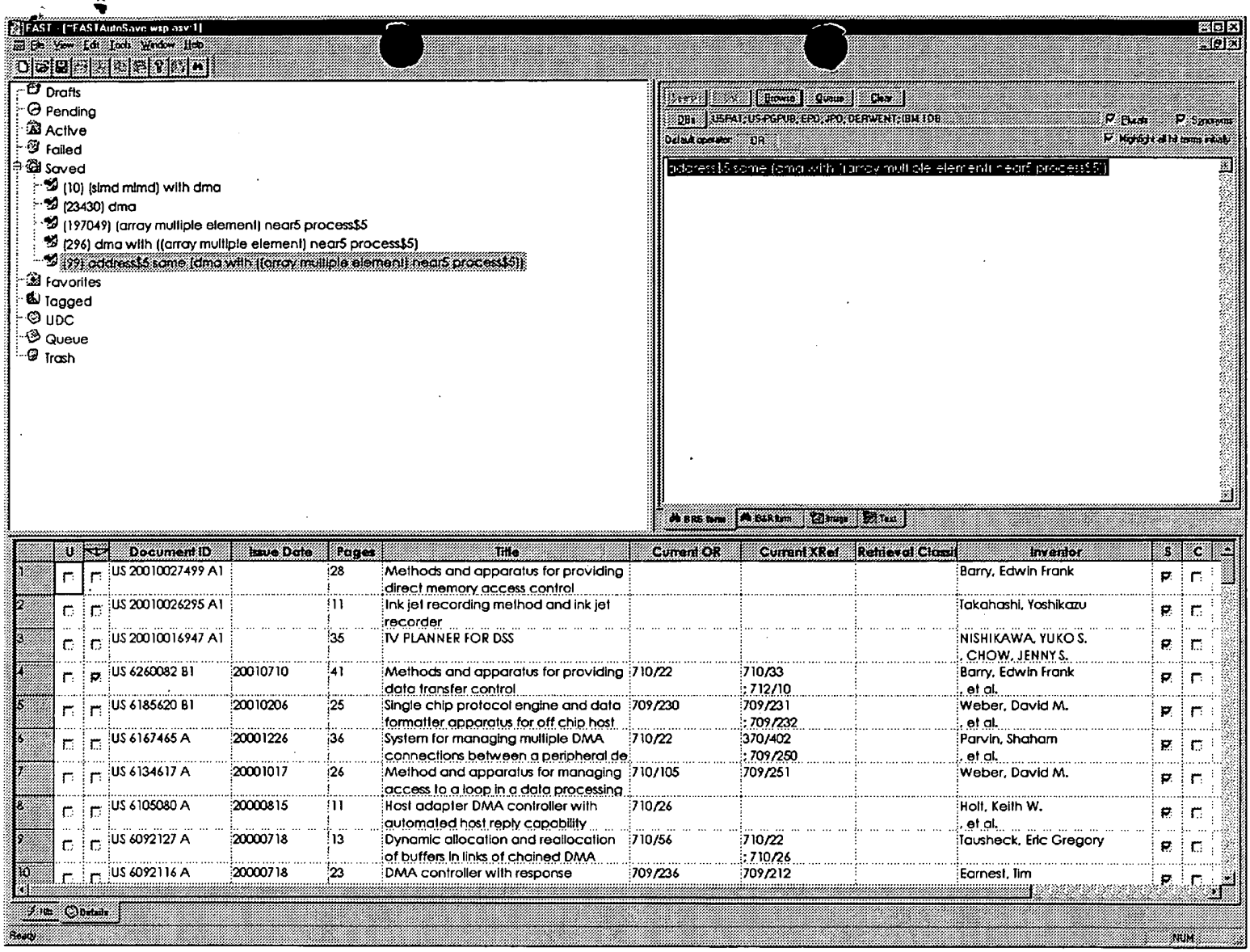
1	☐	☐	US 5418970 A	19950523	31	Parallel processing system with processor array with processing eleme	712/20	709/100 ; 711/6		Gifford, David K.	☑	☐	☐	☐	☐	☐
2	☐	☐	US 5165023 A	19921117	33	Parallel processing system with processor array and network	710/317			Gifford, David K.	☑	☐	☐	☐	☐	☐
3	☐	☐	US 20010027499 A1		28	Methods and apparatus for providing direct memory access control				Barry, Edwin Frank	☑	☐	☐	☐	☐	☐
4	☐	☐	US 6308147 B1	20011023	8	Data structure synthesis in hardware using memory transaction translation	703/25	710/4 ; 711/203		Keaveny, Thomas A.	☑	☐	☐	☐	☐	☐
5	☐	☐	US 6266759 B1	20010724	9	Register scoreboarding to support overlapped execution of vector mem	712/5	712/217		Birrittella, Mark S.	☑	☐	☐	☐	☐	☐
6	☐	☐	US 6256683 B1	20010703	27	Methods and apparatus for providing direct memory access control	710/26	711/203		Barry, Edwin Frank	☑	☐	☐	☐	☐	☐
7	☐	☐	US RE36954 E	20001114	34	SIMD system having logic units arranged in stages of tree structure an	712/11	712/12 ; 712/16		Shindo, Tatsuya , et al.	☑	☐	☐	☐	☐	☐
8	☐	☐	US 6122719 A	20000919	33	Method and apparatus for retiming in a network of multiple context	712/15	709/220 ; 712/11		Mirsky, Ethan , et al.	☑	☐	☐	☐	☐	☐
9	☐	☐	US 6108760 A	20000822	36	Method and apparatus for position independent reconfiguration in a	711/203	711/202 ; 711/204		Mirsky, Ethan , et al.	☑	☐	☐	☐	☐	☐
10	☐	☐	US 6081833 A	20000627	35	Memory space management method.	709/213	709/217		Okamoto, Toshio	☑	☐	☐	☐	☐	☐



	U	KEY	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif	Inventor	S	C
1	☐	☐	US 20010027499 A1		28	Methods and apparatus for providing direct memory access control				Barry, Edwin Frank	☑	☐
2	☐	☐	US 20010026295 A1		11	Ink jet recording method and ink jet recorder				Takahashi, Yoshikazu	☑	☐
3	☐	☐	US 20010016947 A1		35	IV PLANNER FOR DSS				NISHIKAWA, YUKO S. , CHOW, JENNY S.	☑	☐
4	☐	☑	US 6260082 B1	20010710	41	Methods and apparatus for providing data transfer control	710/22	710/33 ; 712/10		Barry, Edwin Frank , et al.	☑	☐
5	☐	☐	US 6185620 B1	20010206	25	Single chip protocol engine and data formatter apparatus for off chip host	709/230	709/231 ; 709/232		Weber, David M. , et al.	☑	☐
6	☐	☐	US 6167465 A	20001226	36	System for managing multiple DMA connections between a peripheral de	710/22	370/402 ; 709/250		Parvin, Shaham , et al.	☑	☐
7	☐	☐	US 6134617 A	20001017	26	Method and apparatus for managing access to a loop in a data processing	710/105	709/251		Weber, David M.	☑	☐
8	☐	☐	US 6105080 A	20000815	11	Host adapter DMA controller with automated host reply capability	710/26			Holt, Keith W. , et al.	☑	☐
9	☐	☐	US 6092127 A	20000718	13	Dynamic allocation and reallocation of buffers in links of chained DMA	710/56	710/22 ; 710/26		Tausheck, Eric Gregory	☑	☐
10	☐	☐	US 6092116 A	20000718	23	DMA controller with response	709/236	709/212		Earnest, Tim	☑	☐

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File View Edit Tools Window Help

- Drafts
- Pending
- Active
  - L1: (22257) dma
  - L2: (28993) direct with memory with access$4) (1
  - L3: (2237) virtual with physical with address$4 with (translat$4 table map$4)
  - L4: (1) ("6260082").PN.
  - L5: (28993) direct with memory with access$4) (1
  - L6: (88) 2 with 3
- Failed
- Saved
- Favorites
- Tagged
- UDC
- Queue
- Trash

DBs: USPAT; EPO; JPO; DERWENT; IBM_TDB

Default operator: OR

Plurals | Synonyms

Highlight all hit terms initially

2 with 3

BRS form | IS&R form | Image | Text

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3		4
1	☐	☐	US 6266285 B1	20010724	32	Method of operating a memory device having write latency	365/194	365/233		Farmwald, Michael, et al.	☑	☐	☐	☐	☐	☐	☐
2	☐	☐	US 6260097 B1	20010710	31	Method and apparatus for controlling a synchronous memory device	710/129	365/233		Farmwald, Michael, et al.	☑	☐	☐	☐	☐	☐	☐
3	☐	☐	US 6185644 B1	20010206	29	Memory system including a plurality of memory devices and a transceiver	710/102	365/189.05; 710/129		Farmwald, Michael, et al.	☑	☐	☐	☐	☐	☐	☐
4	☐	☐	US 6182184 B1	20010130	31	Method of operating a memory device having a variable data input l	710/129	365/233		Farmwald, Michael, et al.	☑	☐	☐	☐	☐	☐	☐
5	☐	☐	US 6178533 B1	20010123	12	Method and system for design verification	714/739	714/32; 714/741		Chang, Lawrence L.	☑	☐	☐	☐	☐	☐	☐
6	☐	☐	US 6128696 A	20001003	32	Synchronous memory device utilizing request protocol and method of	711/105	365/189.02; 365/233		Farmwald, Michael, et al.	☑	☐	☐	☐	☐	☐	☐
7	☐	☐	US 6101152 A	20000808	30	Method of operating a synchronous memory device	365/233	365/194		Farmwald, Michael, et al.	☑	☐	☐	☐	☐	☐	☐
8			US 6092124 A	20000718	11	Method and apparatus for	710/23	710/33		Priem, Curtis							

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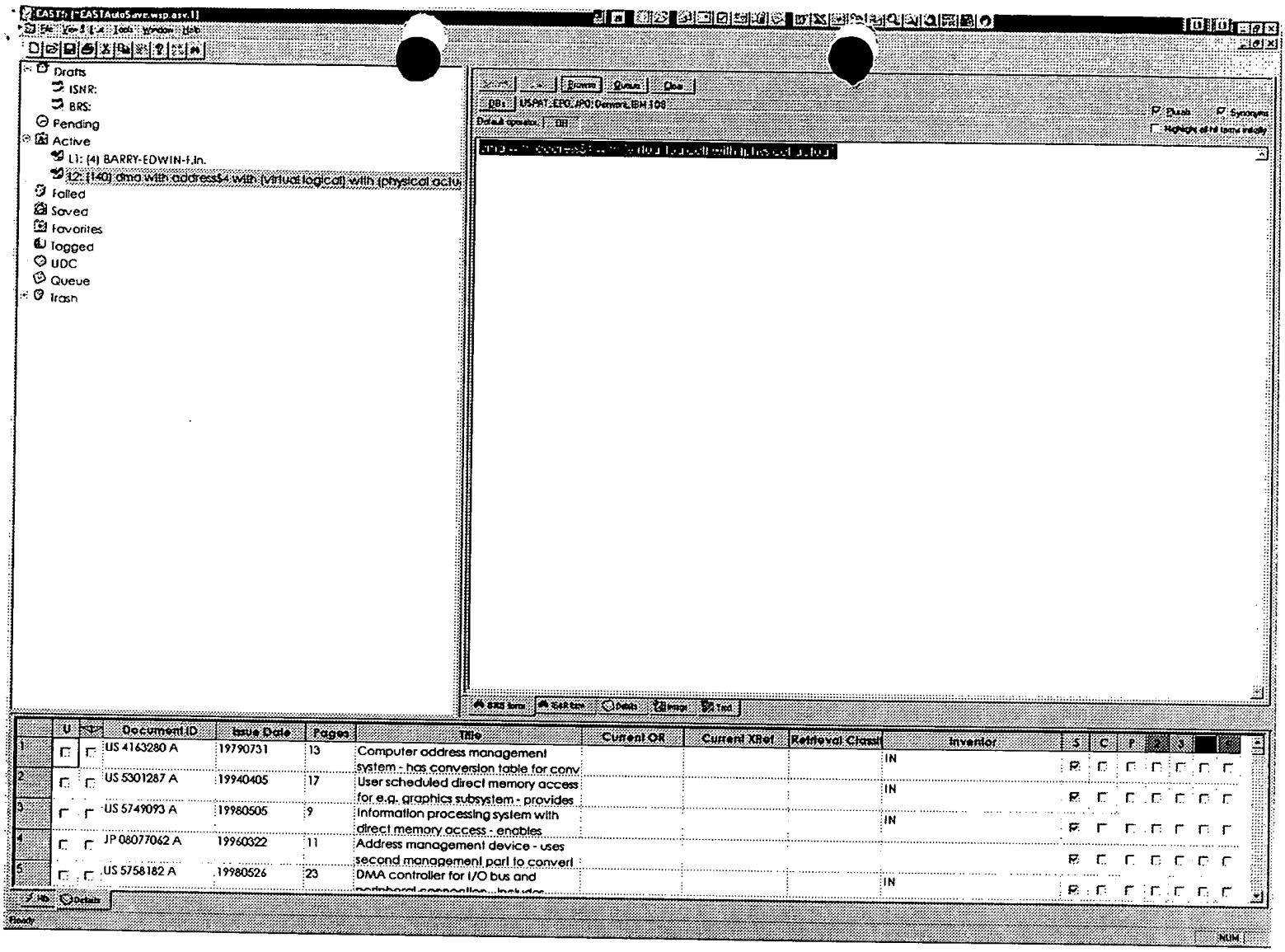
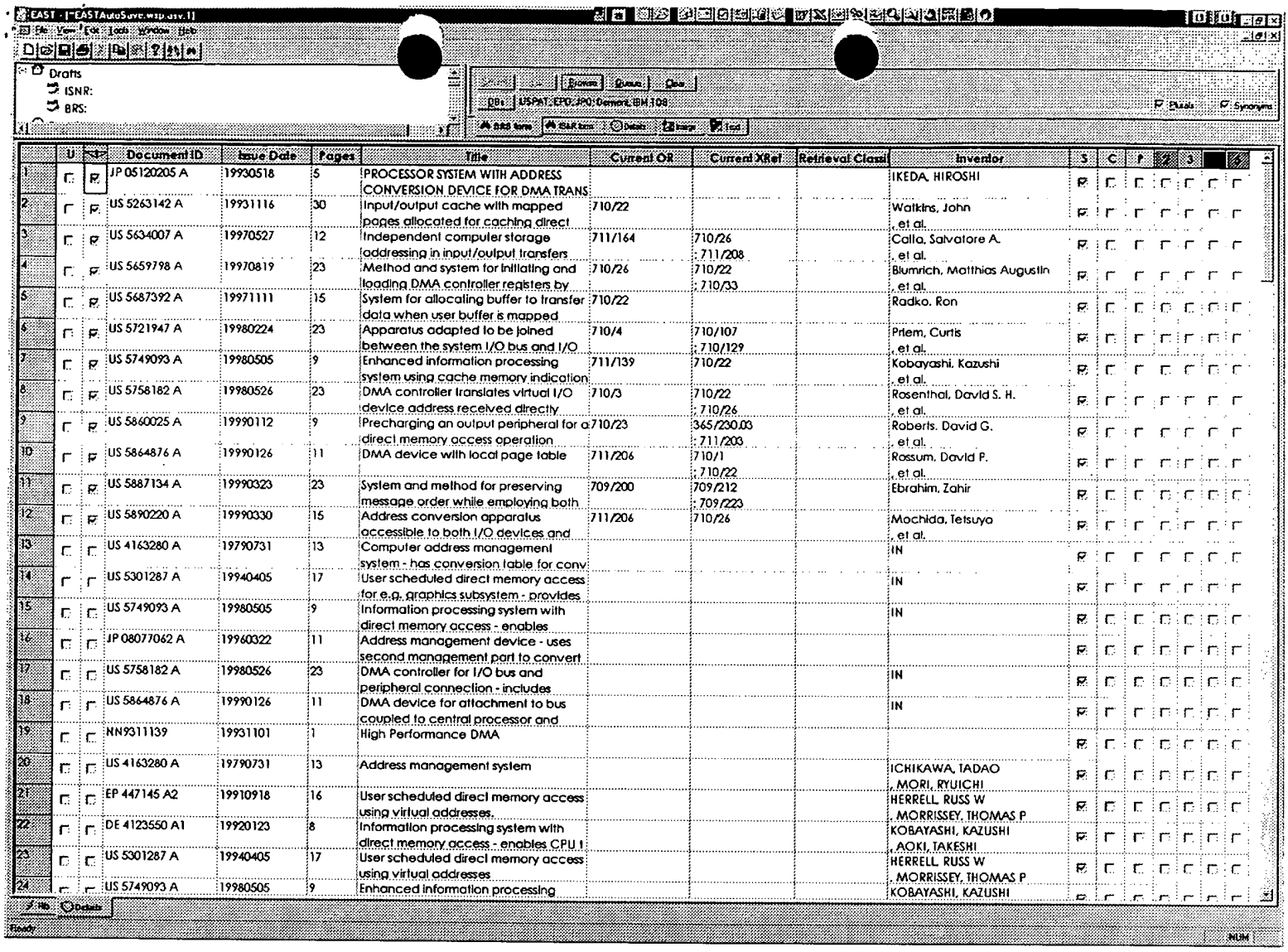


	U		Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif	Inventor	S	C	P	A	J		E
1	☐	☐	US 4163280 A	19790731	13	Computer address management system - has conversion table for conv				IN	☑	☐	☐	☐	☐	☐	☐
2	☐	☐	US 5301287 A	19940405	17	User scheduled direct memory access for e.g. graphics subsystem - provides				IN	☑	☐	☐	☐	☐	☐	☐
3	☐	☐	US 5749093 A	19980505	9	Information processing system with direct memory access - enables				IN	☑	☐	☐	☐	☐	☐	☐
4	☐	☐	JP 08077062 A	19960322	11	Address management device - uses second management part to convert					☑	☐	☐	☐	☐	☐	☐
5	☐	☐	US 5758182 A	19980526	23	DMA controller for I/O bus and peripheral compatible - includes				IN	☑	☐	☐	☐	☐	☐	☐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1	☐	☑	JP 05120205 A	19930518	5	PROCESSOR SYSTEM WITH ADDRESS CONVERSION DEVICE FOR DMA TRANS				IKEDA, HIROSHI	☑	☐	☐	☐	☐	☐	☐
2	☐	☑	US 5263142 A	19931116	30	Input/output cache with mapped pages allocated for caching direct	710/22			Watkins, John , et al.	☑	☐	☐	☐	☐	☐	☐
3	☐	☑	US 5634007 A	19970527	12	Independent computer storage addressing in input/output transfers	711/164	710/26 ; 711/208		Calla, Salvatore A. , et al.	☑	☐	☐	☐	☐	☐	☐
4	☐	☑	US 5659798 A	19970819	23	Method and system for initiating and loading DMA controller registers by	710/26	710/22 ; 710/33		Blumrich, Matthias Augustin , et al.	☑	☐	☐	☐	☐	☐	☐
5	☐	☑	US 5687392 A	19971111	15	System for allocating buffer to transfer data when user buffer is mapped	710/22			Radko, Ron	☑	☐	☐	☐	☐	☐	☐
6	☐	☑	US 5721947 A	19980224	23	Apparatus adapted to be joined between the system I/O bus and I/O	710/4	710/107 ; 710/129		Priem, Curtis , et al.	☑	☐	☐	☐	☐	☐	☐
7	☐	☑	US 5749093 A	19980505	9	Enhanced information processing system using cache memory indication	711/139	710/22		Kobayashi, Kazushi , et al.	☑	☐	☐	☐	☐	☐	☐
8	☐	☑	US 5758182 A	19980526	23	DMA controller translates virtual I/O device address received directly	710/3	710/22 ; 710/26		Rosenthal, David S. H. , et al.	☑	☐	☐	☐	☐	☐	☐
9	☐	☑	US 5860025 A	19990112	9	Precharging an output peripheral for a direct memory access operation	710/23	365/230.03 ; 711/203		Roberts, David G. , et al.	☑	☐	☐	☐	☐	☐	☐
10	☐	☑	US 5864876 A	19990126	11	DMA device with local page table	711/206	710/1 ; 710/22		Rossum, David P. , et al.	☑	☐	☐	☐	☐	☐	☐
11	☐	☑	US 5887134 A	19990323	23	System and method for preserving message order while employing both	709/200	709/212 ; 709/223		Ebrahim, Zahir	☑	☐	☐	☐	☐	☐	☐
12	☐	☑	US 5890220 A	19990330	15	Address conversion apparatus accessible to both I/O devices and	711/206	710/26		Mochida, Tetsuyo , et al.	☑	☐	☐	☐	☐	☐	☐
13	☐	☐	US 4163280 A	19790731	13	Computer address management system - has conversion table for conv				IN	☑	☐	☐	☐	☐	☐	☐
14	☐	☐	US 5301287 A	19940405	17	User scheduled direct memory access for e.g. graphics subsystem - provides				IN	☑	☐	☐	☐	☐	☐	☐
15	☐	☐	US 5749093 A	19980505	9	Information processing system with direct memory access - enables				IN	☑	☐	☐	☐	☐	☐	☐
16	☐	☐	JP 08077062 A	19960322	11	Address management device - uses second management part to convert					☑	☐	☐	☐	☐	☐	☐
17	☐	☐	US 5758182 A	19980526	23	DMA controller for I/O bus and peripheral connection - includes				IN	☑	☐	☐	☐	☐	☐	☐
18	☐	☐	US 5864876 A	19990126	11	DMA device for attachment to bus coupled to central processor and				IN	☑	☐	☐	☐	☐	☐	☐
19	☐	☐	NN9311139	19931101	1	High Performance DMA					☑	☐	☐	☐	☐	☐	☐
20	☐	☐	US 4163280 A	19790731	13	Address management system				ICHIKAWA, TADAO , MORI, RYUICHI	☑	☐	☐	☐	☐	☐	☐
21	☐	☐	EP 447145 A2	19910918	16	User scheduled direct memory access using virtual addresses.				HERRELL, RUSS W , MORRISSEY, THOMAS P	☑	☐	☐	☐	☐	☐	☐
22	☐	☐	DE 4123550 A1	19920123	8	Information processing system with direct memory access - enables CPU t				KOBAYASHI, KAZUSHI , AOKI, TAKESHI	☑	☐	☐	☐	☐	☐	☐
23	☐	☐	US 5301287 A	19940405	17	User scheduled direct memory access using virtual addresses				HERRELL, RUSS W , MORRISSEY, THOMAS P	☑	☐	☐	☐	☐	☐	☐
24	☐	☐	US 5749093 A	19980505	9	Enhanced information processing				KOBAYASHI, KAZUSHI	☑	☐	☐	☐	☐	☐	☐

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DBs USPAT, EPO, JPO, Derwent, IBM_TDB

Pluals Synonyms

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	U		Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Class	Inventor	S	C	P	?	3		
41	☐	☐	US 4163280 A	19790731	13	Address management system	711/207	711/2		Mori, Ryuichi , et al.	☑	☐	☐	☐	☐	☐	☐
42	☐	☐	US 4245305 A	19810113	12	Direct memory access control device	710/25			Gechele, Walter , et al.	☑	☐	☐	☐	☐	☐	☐
43	☐	☐	US 4564900 A	19860114	48	Multiprocessor computer system	709/212	709/213 ; 709/215		Smith, Asbjorn	☑	☐	☐	☐	☐	☐	☐
44	☐	☐	US 4651316 A	19870317	50	Data link extension for data communication networks	370/462	359/118 ; 359/136		Kocan, Kristin F. , et al.	☑	☐	☐	☐	☐	☐	☐
45	☐	☐	US 4888691 A	19891219	42	Method for disk I/O transfer	714/15	710/22 ; 711/111		George, Paul L. , et al.	☑	☐	☐	☐	☐	☐	☐
46	☐	☐	US 4926315 A	19900515	750	Digital data processor with fault tolerant peripheral bus communicatio	714/43	710/128 ; 710/129		Long, William L. , et al.	☑	☐	☐	☐	☐	☐	☐
47	☐	☐	US 4926322 A	19900515	28	Software emulation of bank-switched memory using a virtual DOS monitor	703/23			Slimac, Gary A. , et al.	☑	☐	☐	☐	☐	☐	☐
48	☐	☐	US 4931922 A	19900605	57	Method and apparatus for monitoring peripheral device communications	714/9			Baty, Kurt F. , et al.	☑	☐	☐	☐	☐	☐	☐
49	☐	☐	US 4939643 A	19900703	60	Fault tolerant digital data processor with improved bus protocol	714/9			Long, William L. , et al.	☑	☐	☐	☐	☐	☐	☐
50	☐	☐	US 4959770 A	19900925	12	Data processing system employing two address translators, allowing rapid	711/203	711/206		Kondo, Megumu , et al.	☑	☐	☐	☐	☐	☐	☐
51	☐	☐	US 4974144 A	19901127	57	Digital data processor with fault-tolerant peripheral interface	710/128	714/4		Long, William L. , et al.	☑	☐	☐	☐	☐	☐	☐
52	☐	☐	US 4974150 A	19901127	60	Fault tolerant digital data processor with improved input/output	714/1			Long, William F. , et al.	☑	☐	☐	☐	☐	☐	☐
53	☐	☐	US 5161162 A	19921103	30	Method and apparatus for system bus testability through loopback	714/43	714/716		Watkins, John , et al.	☑	☐	☐	☐	☐	☐	☐
54	☐	☐	US 5208915 A	19930504	19	Apparatus for the microprogram control of information transfer and a	710/22			Stodimeier, Hans , et al.	☑	☐	☐	☐	☐	☐	☐
55	☐	☐	US 5243703 A	19930907	25	Apparatus for synchronously generating clock signals in a data	713/400			Farmwald, Michael , et al.	☑	☐	☐	☐	☐	☐	☐
56	☐	☐	US 5247648 A	19930921	33	Maintaining data coherency between a central cache, an I/O cache and a	711/143	711/119 ; 711/170		Watkins, John , et al.	☑	☐	☐	☐	☐	☐	☐
57	☐	☐	US 5301287 A	19940405	17	User scheduled direct memory access using virtual addresses	711/202	707/104		Herrell, Russ W. , et al.	☑	☐	☐	☐	☐	☐	☐
58	☐	☐	US 5319755 A	19940607	564	Integrated circuit I/O using high performance bus interface	710/104			Farmwald, Michael , et al.	☑	☐	☐	☐	☐	☐	☐
59	☐	☐	US 5347634 A	19940913	12	System and method for directly executing user DMA instruction from us	345/511	222/500		Herrell, Russ W. , et al.	☑	☐	☐	☐	☐	☐	☐
60	☐	☐	US 5392393 A	19950221	13	Architecture for a high performance three dimensional graphics	345/505	345/419 ; 345/503		Deering, Michael F.	☑	☐	☐	☐	☐	☐	☐
61	☐	☐	US 5408129 A	19950418	23	Integrated circuit I/O using a high performance bus interface	257/692	257/693 ; 257/786		Farmwald, Michael , et al.	☑	☐	☐	☐	☐	☐	☐
62	☐	☐	US 5408605 A	19950418	23	Command preprocessor for a high performance three dimensional graphi	345/523	345/419		Deering, Michael F.	☑	☐	☐	☐	☐	☐	☐
63	☐	☐	US 5440682 A	19950808	26	Draw processor for a high performance three dimensional graphi	345/503	345/506 ; 345/509		Deering, Michael F.	☑	☐	☐	☐	☐	☐	☐
64	☐	☐	US 5473575 A	19951205	23	Integrated circuit I/O using a high	365/230.06	327/379		Farmwald, Michael	☑	☐	☐	☐	☐	☐	☐

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	U		Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Class	Inventor	S	C	P	2	3		
64			US 5473575 A	19951205	23	Integrated circuit I/O using a high performance bus interface	365/230.06	327/379 ; 327/391		Farmwald, Michael , et al.	☑						
65			US 5487152 A	19960123	78	Method and apparatus for frame header splitting in a media access	709/236	370/438 ; 709/213		Young, Desmond W.	☑						
66			US 5497476 A	19960305	7	Scatter-gather in data processing system	711/112	711/201		Oldfield, Clive S. , et al.	☑						
67			US 5499385 A	19960312	25	Method for accessing and transmitting data to/from a memory in packets	710/3	711/100		Farmwald, Michael , et al.	☑						
68			US 5511166 A	19960423	75	Method and apparatus for receive frame sorting in a media access	709/250			Travaglio, Mark A. , et al.	☑						
69			US 5513320 A	19960430	75	Transmit data descriptor structure in a media access control/host system	709/236	709/213 ; 710/5		Young, Desmond W. , et al.	☑						
70			US 5513327 A	19960430	25	Integrated circuit I/O using a high performance bus interface	710/129	365/189.02 ; 365/230.02		Farmwald, Michael , et al.	☑						
71			US 5517611 A	19960514	29	Floating-point processor for a high performance three dimensional	345/503	345/513		Deering, Michael F.	☑						
72			US 5524230 A	19960604	39	External information storage system with a semiconductor memory	711/103			Sakaue, Yoshinori , et al.	☑						
73			US 5530673 A	19960625	136	Flash memory control method and information processing system therewit	365/185.09	365/185.04 ; 365/185.11		Tobita, Tsunehiro , et al.	☑						
74			US 5530821 A	19960625	9	Method and apparatus including independent virtual address translatio	711/203	711/206 ; 711/207		Miyamoto, Tsuyoshi	☑						
75			US 5574944 A	19961112	15	System for accessing distributed memory by breaking each accepted	710/5	711/153		Stager, Gary B.	☑						
76			US 5600799 A	19970204	75	Status batching and filtering in a media access control/host system	710/100	370/419 ; 370/463		Young, Desmond W. , et al.	☑						
77			US 5606717 A	19970225	25	Memory circuitry having bus interface for receiving information in	710/36	710/10 ; 710/104		Farmwald, Michael , et al.	☑						
78			US 5608869 A	19970304	75	Method and apparatus for reliable descriptor chaining in a media access	709/250	370/463 ; 710/129		Hamstra, James R. , et al.	☑						
79			US 5608891 A	19970304	44	Recording system having a redundant array of storage devices and having	711/114	711/113 ; 714/6		Mizuno, Masahiro , et al.	☑						
80			US 5615392 A	19970325	12	Method and apparatus for consolidated buffer handling for comp	710/56	711/152 ; 711/154		Harrison, David F. , et al.	☑						
81			US 5619651 A	19970408	74	I/O data unit symmetry in a media access control/host system interface	709/250	710/33		Young, Desmond W.	☑						
82			US 5619652 A	19970408	75	Automatic preemption recovery and frame repeat option in a media acces	709/250	370/419 ; 370/463		Travaglio, Mark A. , et al.	☑						
83			US 5623692 A	19970422	23	Architecture for providing input/output operations in a computer	710/3	710/12 ; 710/130		Priem, Curtis , et al.	☑						
84			US 5638334 A	19970610	26	Integrated circuit I/O using a high performance bus interface	365/230.03	365/200 ; 365/207		Farmwald, Michael , et al.	☑						
85			US 5657481 A	19970812	28	Memory device with a phase locked loop circuitry	713/400	327/147 ; 331/2		Farmwald, Michael , et al.	☑						
86			US 5659797 A	19970819	10	Sparc RISC based computer system including a single chip processor with	710/22	710/105 ; 710/26		Zandveld, Frederik , et al.	☑						
87			US 5685011 A	19971104	24	Apparatus for handling failures to	710/3	710/5		Rosenthal, David S. H.							

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	U		Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classi	Inventor	S	C	P	?	3
87	☐	☐	US 5685011 A	19971104	24	Apparatus for handling failures to provide a safe address translation in	710/3	710/5 ; 711/1		Rosenthal, David S. H. , et al.	☑	☐	☐	☐	☐
88	☐	☐	US 5732285 A	19980324	12	Method and apparatus for consolidated buffer handling for comp	710/56	710/52 ; 710/55		Harrison, David Frank , et al.	☑	☐	☐	☐	☐
89	☐	☐	US 5740464 A	19980414	23	Architecture for providing input/output operations in a computer	710/3	710/12 ; 710/130		Priem, Curtis , et al.	☑	☐	☐	☐	☐
90	☐	☐	US 5754764 A	19980519	143	Combination of input output circuitry and local area network systems	709/200	710/5 ; 710/56		Davis, Timothy D. , et al.	☑	☐	☐	☐	☐
91	☐	☐	US 5802576 A	19980901	8	Speculative cache snoop during DMA line update	711/146	711/213		Tzeng, Allan , et al.	☑	☐	☐	☐	☐
92	☐	☐	US 5809263 A	19980915	34	Integrated circuit I/O using a high performance bus interface	710/129	710/126 ; 711/211		Farmwald, Michael , et al.	☑	☐	☐	☐	☐
93	☐	☐	US 5825878 A	19981020	10	Secure memory management unit for microprocessor	713/190	713/193		Takahashi, Richard , et al.	☑	☐	☐	☐	☐
94	☐	☐	US 5841580 A	19981124	30	Integrated circuit I/O using a high performance bus interface	365/194	365/189.12 ; 710/130		Farmwald, Michael , et al.	☑	☐	☐	☐	☐
95	☐	☐	US 5862083 A	19990119	136	Information processing system	365/185.09	365/185.11 ; 365/185.22		Tobita, Tsunehiro , et al.	☑	☐	☐	☐	☐
96	☐	☐	US 5901312 A	19990504	22	Providing application programs with unmediated access to a contested	709/104	709/1		Radko, Ronald O.	☑	☐	☐	☐	☐
97	☐	☐	US 5909546 A	19990601	29	Network interface having support for allowing remote operations with	709/212			Osborne, Randy B.	☑	☐	☐	☐	☐
98	☐	☐	US 5909559 A	19990601	186	Bus bridge device including data bus of first width for a first	710/127	710/129 ; 710/131		So, John Ling Wing	☑	☐	☐	☐	☐
99	☐	☐	US 5915105 A	19990622	32	Integrated circuit I/O using a high performance bus interface	710/129	365/233		Farmwald, Michael , et al.	☑	☐	☐	☐	☐
100	☐	☐	US 5928343 A	19990727	32	Memory module having memory devices containing internal device ID	710/104	710/9		Farmwald, Michael , et al.	☑	☐	☐	☐	☐
101	☐	☐	US 5937436 A	19990810	15	Network interface circuit including an address translation unit and	711/202	711/108 ; 711/135		Watkins, John E.	☑	☐	☐	☐	☐
102	☑	☐	US 5953263 A	19990914		Synchronous memory device having a programmable register and method of	365/194			Farmwald, Michael , et al.	☐	☐	☐	☐	☐
103	☑	☐	US 5954804 A	19990921		Synchronous memory device having an internal register	710/36	710/10 ; 710/107		Farmwald, Michael , et al.	☐	☐	☐	☐	☐
104	☑	☐	US 5973964 A	19991026		Flash memory control method and information processing system therewit	365/185.29	365/185.11 ; 365/189.01		Tobita, Tsunehiro , et al.	☐	☐	☐	☐	☐
105	☑	☐	US 5983332 A	19991109		Asynchronous transfer mode (ATM) segmentation and reassembly unit	711/202	711/203 ; 711/205		Watkins, John E.	☐	☐	☐	☐	☐
106	☑	☐	US 5983320 A	19991109		Method and apparatus for externally configuring and modifying the	711/114	710/51 ; 711/100		Farmwald, Michael , et al.	☐	☐	☐	☐	☐
107	☑	☐	US 5991854 A	19991123		Circuit and method for address translation, using update and flush	711/135	711/207		Watkins, John E.	☐	☐	☐	☐	☐
108	☑	☐	US 6021462 A	20000201		Methods and apparatus for system memory efficient disk access to a raid	711/114	711/111 ; 711/112		Minow, Martin A. , et al.	☐	☐	☐	☐	☐
109	☑	☐	US 6023738 A	20000208		Method and apparatus for accelerating the transfer of graphical i	710/23	710/33 ; 710/56		Priem, Curtis , et al.	☐	☐	☐	☐	☐
110	☐	☐	US 6032214 A	20000229		Method of operating a synchronous	710/129	710/35		Farmwald, Michael	☐	☐	☐	☐	☐

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	U		Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classi	Inventor	S	C	P	2	3		5
110	P		US 6032214 A	20000229		Method of operating a synchronous memory device having a variable dat	710/129	710/35		Farmwald, Michael , et al.							
111	P		US 6032215 A	20000229		Synchronous memory device utilizing two external clocks	710/129	365/189.02 ; 365/230.02		Farmwald, Michael , et al.							
112	P		US 6035365 A	20000307		Dual clocked synchronous memory device having a delay time register a	710/129	365/230.03		Farmwald, Michael , et al.							
113	P		US 6034918 A	20000307		Method of operating a memory having a variable data output length	365/233			Farmwald, Michael , et al.							
114	P		US 6038195 A	20000314		Synchronous memory device having a delay time register and method of	365/233	365/194 ; 713/401		Farmwald, Michael , et al.							
115	P		US 6044426 A	20000328	33	Memory system having memory devices each including a programma	710/104	711/170		Farmwald, Michael , et al.							
116	P		US 6047335 A	20000404	10	Video display device applied for a graphics accelerator	710/22	345/501 ; 711/203		Takizawa, Tetsuro							
117	P		US 6047307 A	20000404	22	Providing application programs with unmediated access to a contested	709/100	709/104		Radko, Ronald O.							
118	P		US 6049857 A	20000411	19	Apparatus and method for translating addresses utilizing an ATU	711/207	711/135 ; 711/163		Watkins, John E.							
119	P		US 6049846 A	20000411	30	Integrated circuit having memory which synchronously samples informati	710/126	713/500		Farmwald, Michael , et al.							
120	P		US 6058437 A	20000502	10	D.M.A. device that handles cache misses by managing an address of an	710/22	345/511 ; 709/212		Park, Jun Hee , et al.							
121	P		US 6065071 A	20000516	18	Method and apparatus for trapping unimplemented operations in	710/22	710/52 ; 710/57		Priem, Curtis , et al.							
122	P		US 6067592 A	20000523	32	System having a synchronous memory device	710/104	713/400		Farmwald, Michael , et al.							
123	P		US 6070222 A	20000530	34	Synchronous memory device having identification register	711/105	365/189.02 ; 365/230.02		Farmwald, Michael , et al.							
124	P		US 6073224 A	20000606	15	Network interface circuit with replacement circuitry and method for	711/202	711/133 ; 711/207		Watkins, John E.							
125	P		US 6075938 A	20000613	15	Virtual machine monitors for scalable multiprocessors	703/27	709/214 ; 709/321		Bugnion, Edouard , et al.							
126	P		US 6078733 A	20000620	35	Network interface having support for message processing and an interface	709/250	709/212 ; 709/216		Osborne, Randy B.							
127	P		US 6078559 A	20000620	20	Optical disk having read-only and rewritable areas with overlapping	369/275.3	369/275.1		Takemura, Yoshinari , et al.							
128	P		US 6078520 A	20000620	136	Flash memory control method and information processing system therewit	365/185.09	365/185.11 ; 365/185.29		Tobita, Tsunehiro , et al.							
129	P		US 6081854 A	20000627	24	System for providing fast transfers to input/output device by assuring	710/37	710/12 ; 710/5		Priem, Curtis , et al.							
130	P		US 6085284 A	20000704	32	Method of operating a memory device having a variable data output	711/105	365/189.02 ; 365/230.02		Farmwald, Michael , et al.							
131	P		US 6092124 A	20000718	11	Method and apparatus for accelerating the rendering of images	710/23	710/33 ; 710/52		Priem, Curtis , et al.							
132	P		US 6101152 A	20000808	30	Method of operating a synchronous memory device	365/233	365/194		Farmwald, Michael , et al.							
133	P		US 6105119 A	20000815	188	Data transfer circuitry, DSP wrapper	711/219	710/129		Kerr, Jeffrey L.							

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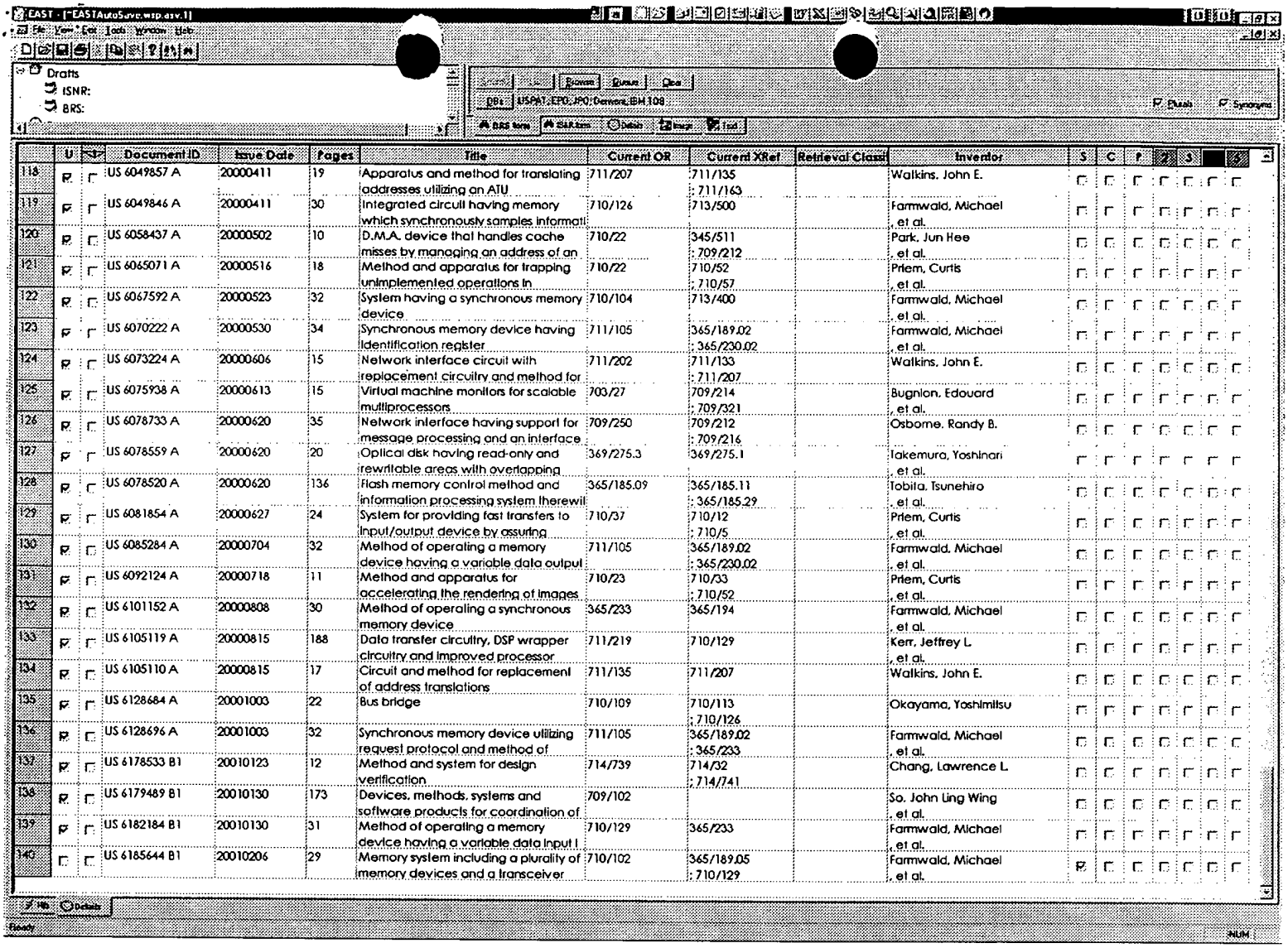

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	U		Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3		
118	☑	☐	US 6049857 A	20000411	19	Apparatus and method for translating addresses utilizing an ATU	711/207	711/135 ; 711/163		Watkins, John E.	☐	☐	☐	☐	☐	☐	☐
119	☑	☐	US 6049846 A	20000411	30	Integrated circuit having memory which synchronously samples informati	710/126	713/500		Farmwald, Michael , et al.	☐	☐	☐	☐	☐	☐	☐
120	☑	☐	US 6058437 A	20000502	10	D.M.A. device that handles cache misses by managing an address of an	710/22	345/511 ; 709/212		Park, Jun Hee , et al.	☐	☐	☐	☐	☐	☐	☐
121	☑	☐	US 6065071 A	20000516	18	Method and apparatus for trapping unimplemented operations in	710/22	710/52 ; 710/57		Priem, Curtis , et al.	☐	☐	☐	☐	☐	☐	☐
122	☑	☐	US 6067592 A	20000523	32	System having a synchronous memory device	710/104	713/400		Farmwald, Michael , et al.	☐	☐	☐	☐	☐	☐	☐
123	☑	☐	US 6070222 A	20000530	34	Synchronous memory device having identification register	711/105	365/189.02 ; 365/230.02		Farmwald, Michael , et al.	☐	☐	☐	☐	☐	☐	☐
124	☑	☐	US 6073224 A	20000606	15	Network interface circuit with replacement circuitry and method for	711/202	711/133 ; 711/207		Watkins, John E.	☐	☐	☐	☐	☐	☐	☐
125	☑	☐	US 6075938 A	20000613	15	Virtual machine monitors for scalable multiprocessors	703/27	709/214 ; 709/321		Bugnion, Edouard , et al.	☐	☐	☐	☐	☐	☐	☐
126	☑	☐	US 6078733 A	20000620	35	Network interface having support for message processing and an interface	709/250	709/212 ; 709/216		Osborne, Randy B.	☐	☐	☐	☐	☐	☐	☐
127	☑	☐	US 6078559 A	20000620	20	Optical disk having read-only and rewritable areas with overlapping	369/275.3	369/275.1		Takemura, Yoshinori , et al.	☐	☐	☐	☐	☐	☐	☐
128	☑	☐	US 6078520 A	20000620	136	Flash memory control method and information processing system therewit	365/185.09	365/185.11 ; 365/185.29		Tobita, Tsunehiro , et al.	☐	☐	☐	☐	☐	☐	☐
129	☑	☐	US 6081854 A	20000627	24	System for providing fast transfers to input/output device by assuring	710/37	710/12 ; 710/5		Priem, Curtis , et al.	☐	☐	☐	☐	☐	☐	☐
130	☑	☐	US 6085284 A	20000704	32	Method of operating a memory device having a variable data output	711/105	365/189.02 ; 365/230.02		Farmwald, Michael , et al.	☐	☐	☐	☐	☐	☐	☐
131	☑	☐	US 6092124 A	20000718	11	Method and apparatus for accelerating the rendering of images	710/23	710/33 ; 710/52		Priem, Curtis , et al.	☐	☐	☐	☐	☐	☐	☐
132	☑	☐	US 6101152 A	20000808	30	Method of operating a synchronous memory device	365/233	365/194		Farmwald, Michael , et al.	☐	☐	☐	☐	☐	☐	☐
133	☑	☐	US 6105119 A	20000815	188	Data transfer circuitry, DSP wrapper circuitry and improved processor	711/219	710/129		Kerr, Jeffrey L. , et al.	☐	☐	☐	☐	☐	☐	☐
134	☑	☐	US 6105110 A	20000815	17	Circuit and method for replacement of address translations	711/135	711/207		Watkins, John E.	☐	☐	☐	☐	☐	☐	☐
135	☑	☐	US 6128684 A	20001003	22	Bus bridge	710/109	710/113 ; 710/126		Okayama, Yoshimitsu	☐	☐	☐	☐	☐	☐	☐
136	☑	☐	US 6128696 A	20001003	32	Synchronous memory device utilizing request protocol and method of	711/105	365/189.02 ; 365/233		Farmwald, Michael , et al.	☐	☐	☐	☐	☐	☐	☐
137	☑	☐	US 6178533 B1	20010123	12	Method and system for design verification	714/739	714/32 ; 714/741		Chang, Lawrence L.	☐	☐	☐	☐	☐	☐	☐
138	☑	☐	US 6179489 B1	20010130	173	Devices, methods, systems and software products for coordination of	709/102			So, John Ling Wing , et al.	☐	☐	☐	☐	☐	☐	☐
139	☑	☐	US 6182184 B1	20010130	31	Method of operating a memory device having a variable data input l	710/129	365/233		Farmwald, Michael , et al.	☐	☐	☐	☐	☐	☐	☐
140	☐	☐	US 6185644 B1	20010206	29	Memory system including a plurality of memory devices and a transceiver	710/102	365/189.05 ; 710/129		Farmwald, Michael , et al.	☑	☐	☐	☐	☐	☐	☐

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